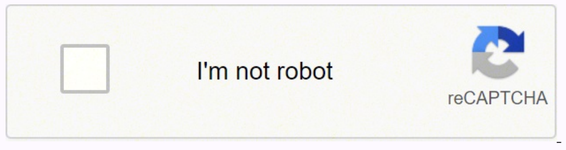

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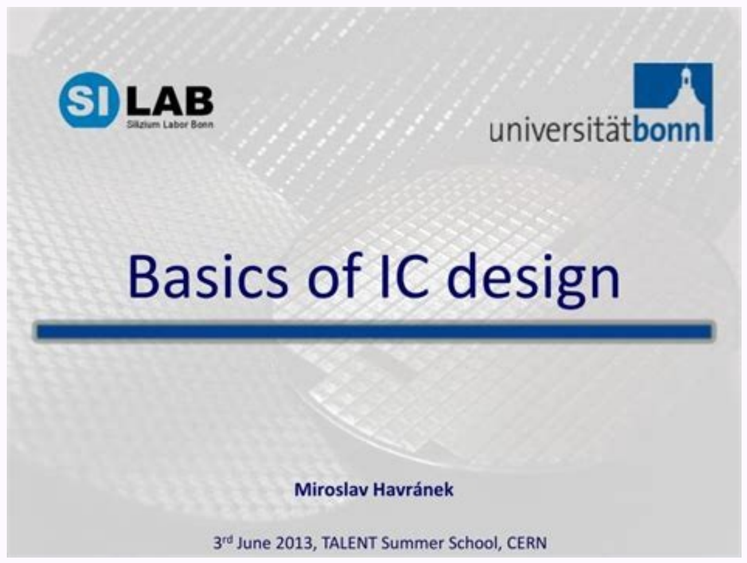

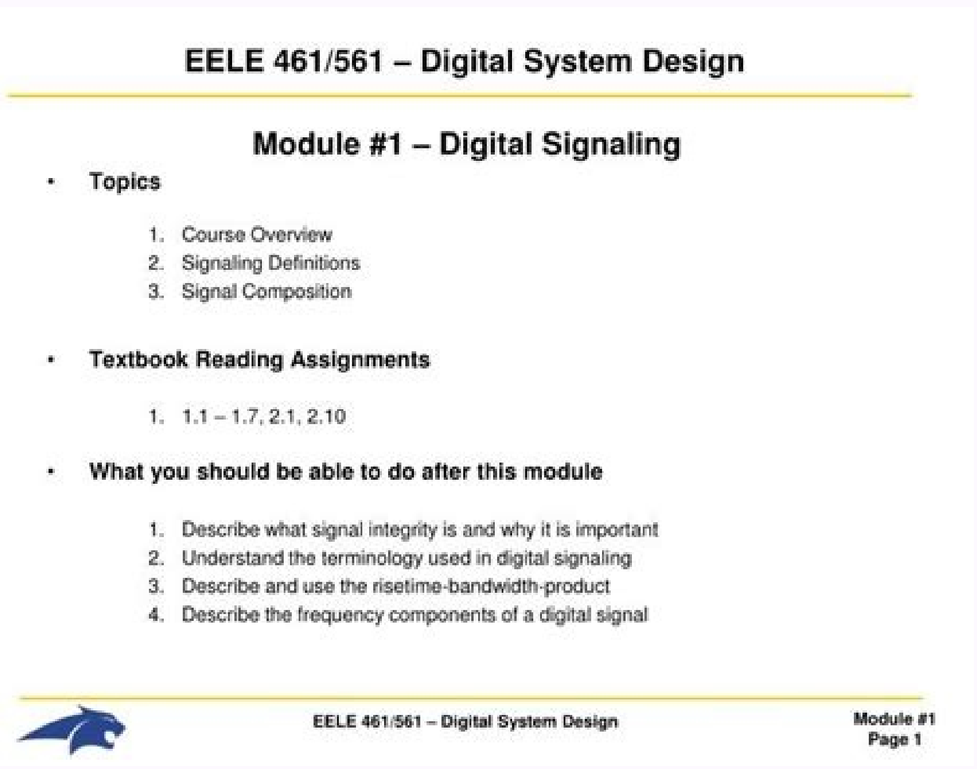

EELE 461/561 – Digital System Design

Module #1 – Digital Signaling

- Topics
  1. Course Overview
  2. Signaling Definitions
  3. Signal Composition
- **Textbook Reading Assignments**
  1. 1.1 – 1.7, 2.1, 2.10
- **What you should be able to do after this module**
  1. Describe what signal integrity is and why it is important
  2. Understand the terminology used in digital signaling
  3. Describe and use the risetime-bandwidth-product
  4. Describe the frequency components of a digital signal

EELE 461/561 – Digital System Design — Module #1 Page 1

Surface Traveling Wave Effect in Radar Images of Turntable

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Abstract

The turntable is an important element of ISAR imaging. It must contribute negligibly to the RCS of the Object-Under-Test that is placed upon it. The turntable used at the NFDRF Radar Cross-Section Range at Jodhpur is a rigid metal circular structure of 8.0 m diameter capable of supporting a payload of 40 tons, and installed flush with ground surface. The turntable construction uses a number of countersunk fasteners to attach the tabletop onto the structural framework, so that the tabletop itself is free of protrusions.

As the turntable's contribution to the ISAR image of the Object-under-test should be minimal, a Near-Field Imaging study of the turntable response has been carried out. The study has been carried out in X-band (9–11 GHz), for both Horizontal and Vertical polarizations. Antennas are mounted at approx 30m from the center of the turn table. It is observed that all the fasteners on the table show up prominently when imaged with vertically polarized excitation, while they are totally absent in images created using horizontally polarized excitation. To investigate further, one radial row of fasteners is covered with conducting tape. It is observed that the contribution of this row then disappears from the Vertically Polarized image also.

These results originate from the effects of surface traveling waves. Surface traveling waves are introduced only when there is a component of the incident electric field tangential to the surface and in the plane of incidence. The electric field component induces surface currents that flow along the body in the longitudinal direction. Whenever these currents encounter a geometrical or impedance discontinuity, they are partly reflected back towards the direction of incidence. Here, the surface traveling waves are generated on the turntable in vertical polarization mode only as table is horizontal. The radar images of the turntable clearly demonstrate this surface traveling effect by showing up the fastener discontinuities in response to vertically polarized incident radiation.

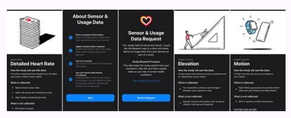
Keywords: Surface Traveling Wave, RCS, ISAR Imaging.

1. Introduction

High Resolution Radar images of the Object-Under-Test (OUT) are generated by ISAR measurements. The OUT is deployed on a precision azimuth positioner and backscatter data are acquired over multiple aspects and frequencies. These multi-aspect and multi-frequency data are processed to form high-resolution images of the Object-Under-Test.

The NFDRF (Near-Field Diagnostic RCS Facility) at Jodhpur has the capability of carrying out 2D SAR and ISAR imaging of large targets. For ISAR measurements, a large Positioner is installed such that its Turntable, which is of 8 m diameter, is flush with the ground surface. It is capable of handling a load of 40 tons, and provides servo-controlled positioning accuracy of +/- 0.5 degree.

As the OUT reflections are the prime data of interest, we would like the reflections contributed by the background to be minimal. The reflections associated with the turntable have been measured to evaluate this background signature, for both Horizontal and Vertical Polarizations.



The tension tensioning that develops in the gate and the substrate of a mosfet during plasma processing basically comes from three sources. For a given antenna proposal, a larger tunneling current is supported when plasma density is higher. The first has a violation of the antenna and the second number. Charging filtering (shading) due to microscrepic topography on the cookie. Figure: The insertion of the jumper breaks a long wire in most tools, the insertion of the jumper is automatically performed during routing. If the connection with the silent does not exist, the charges and may accumulate in interconnecting to the point where the ruffled discharge occurs and the permanent results of fanic damage, for example, for those Mosfet holder. During metallic (when the methanlic wires are placed between the devices), some wires connected to the transistor polysylter ports can be left floating (disconnected) that the upper metal layers are deposited. It allows the super control of the pattern (modeler edges / less below the cloth) and also allows you to be quantic reactions that are not possible in the traditional gap (ãºmida). The most important mothers are the insertion of the jumper and the diode insertion to remove the violation of the antenna. Distribution does not uniform of the plastic potential throughout the cracker. Effects of Ca due to the nature of the RF discharge that support the plasma. Antenna rules are commonly expressed as a wire area proposal over the door (AW/AG) for each metal layer and cut (via). Jumper insertion: a jumper is a forceful layer change from one metal to another and then returns to the same layer. The proposal of the driver's area to the Ã³xide under the gate is the proposal of the antenna. This is the so -called "previous effect". The disadvantage is that it can potentially contribute to the routing of ,snoÃ ,snoÃ ed oxulf oa laugi res o£Ân edop snort©Âle ed oxulf o ,agrac ad odlas od o£Ã§Âidnoc ad odnednepeD .asrever anetna ad sotiefe sod sTEFN od amelborp o euq od sievÃtecsus siam sTEFP .roirepus latem ed sadamac san otnemanoitsegnoc ed There is a positive or negative net collection rate. The antenna checker is called for each pin in question to decide first, if the pin has antenna violations and second, if a jumper failed in the pin area because the area is blocked and a large enough hole does not exist. Figure of the insertion of the diode: inserted near a logic Door Input Pin As shown in Figure, the diode insert near a logical gate input pin on a network provides a discharge path to the substrate so that the embedded loads cannot damage the transistor gate. When you run these commands, the tool detects and fixes antenna breaches using jumpers and a ripup strategy and adapted redirection. The process is non-destructive, and it is possible that the network can download through the diode several times during the manufacturing process. The reason of the antenna, in a rough sense, is a current multiplier that amplifies the density of tunnel current through the gate oxide. During the normal chip operation, the reverse bias prevents electrons from flowing from the network through the diode and the chip substrate. Then by adjusting the physical layout of the interconnections, the antenna reasons can be reduced to an acceptable level. After detailed routing, you can fix antenna violations manually by inserting jumpers using commands corresponding to the tool you are using. In this process, the metal sides are protected, so that the rules of the antenna need to be based on the top surface of the metal. Fictitious Transistors The addition of extra gates will reduce the capacitance ratio. When this gradient becomes large enough, it is relieved by an explosive discharge (i.e. "illumination"). This voltage is greater than normal operating voltage, but less than the voltage at which an electrostatic discharge at the gate can be omoC omoC .otnemagerrac ed onad o ©Ã seled mU .acig3Âl atrop ad adartne ed agrac ad otnemua oa odived opmet o asarta e ahlip ad aer¡Ã a atnemua odoid ed o£ÂÃ§ÂÃresni a ,etnemzilefnI result a voltage gradient develops through the gate oxide. When it is eventually connected through the "top-level metal point", it is no longer exposed to load buildup and again does not contribute to an antenna breach. This example shows that antenna violations can be avoided by using jumpers (also known as “bridge”). A number of techniques can be used to minimize the effect of the antenna. The semiconductor manufacturer usually provides the gate area or the size, and the antenna tester calculates the appropriate wire area using the wire accumulation method (load) specified by the manufacturer. Antenna Effects: Modern wafer processing uses ‘Plasma etch’ (or ‘dry etch’). They, however, add to the magnitude of stress tensions developed by non-uniform plasma potential or topographical load filtration or the sum of both. In other words, the "antena" is an interconnection, i.e. a conductor such as polysilicon or metal, which is not electrically connected to silicon, i.e. not "encalated", during the processing stages of the cookie. Both plasma electrons and positive ions are impinginging on the exposed conductor during processing. To avoid antenna problems, you should design all net topologies so that no gate is vulnerable to a large amount of floating load. During manufacturing, however, the load on the network can build to the point where the voltage drop through the diode exceeds its rupture voltage. The substrate remains on the ground as it is connected to the manufacturing device. The insertion of the diode can repair the remaining antenna problems. The available loads are the liquid loads collected from the plasma by the driver exposed with connection to the gate or substrate. Voltage voltages due to AC effects are quite small in most cases and cannot causeby themselves. Antenna rule

verification is different for each process technology because the whole to express to express ratio is not standardized. In most of the tools, diode insertion is performed automatically when you use the routing command. For example, there can be too much congestion to insert a jumper or the diffusion strengths of the output pins are too weak. (This is usually referred as ¢ÃÂÂcharge-collecting antenna problem¢ÃÂÂ or simply antenna problem) Most important ways to repair the antenna violation: Using jumpers to break up long wires connected to gates (Jumpers are a short metal segment inserted onto a long route of another metal layer). The top of the metal is protected by a resist during this step, so the antenna rules for this process should be based on the metal sidewall area. The collected net charges are channeled to the gate as shown in fig. Clearly, the size of the conductor exposed to the plasma plays a role in determining the magnitude of the net charge collection rate and therefore the tunneling current. The Importance of Jumper Location in Repairing Antenna Violations Figure shows two nets with the same separation between the input and output pins, but slightly different jumper locations. The problem is more significant at smaller technologies because the damage resulting from the discharge is more likely to extend across the entire length of the gate. 'Antenna ratio' is defined as the ratio between the physical area of the conductors making up the antenna to the total gate oxide area to which the antenna is electrically connected. Design Solution to reduce Antenna Effects: Router options Break signal wires and route to upper metal layers by jumper insertion All metal being etched is not connected to a gate until the last metal layer is etched. When this metal layer is fabricated, the long piece on one side is no longer electrically connected to the gate and does not contribute to any antenna effects. The amount of charge that builds up depends on a number of factors; the most important from an antenna is how much metal is exposed. Unfortunately, the use of jumpers can only diffuse the antenna problem to the higher metal layer of the jumper, where antennainfections can still occur because all the geometries of the network they are physically connected with each other. Simplification: The load builds (DC) on the metal wires (antenna) during application of plasma etch Because the gate of a MOSFET is like a capacitor If the potential at the gate reaches a certain value, it will ‘break’ "Punch through" occurs The gate is irreparably damaged The ' antenna reason' of an interconnect is used to predict whether the antenna effect will occur. In an aluminum-based process, the load buildup occurs during the ETCH stage. The built-in protection diode Connect reversing biased diodes to the transistor gate (during normal circuit operation, the diode does not affect functionality). This destructive phenomenon is known as the " antenna effect". The factors that these rules need to consider is whether the antenna should be based on the "top" area of metal or in its "sidewall" area. A long floating interconnection (without a suitable oxide shielding layer) can act as a temporary capacitor, collecting loads during manufacturing steps, such as plasma recording. This antenna effect can be understood in a different way too. Figure: Impact of jumper location The difference is that the first network has a long metal connection1 for the input pin. A diode can be used to protect all input ports that are connected to the same output ports. You can manually insert diodes using the corresponding tool commands. A higher proportion implies a greater propensity to fail due to the effect of the antenna. 1 where it is neutralized by the current tunnel through the gate-oxide. Inserting diodes after detailed placement After detailed routing, antenna violations etneper etneper ed ©Ã etnautulf ³Ãn o erbos adÃurtsnoc aigrene a eS .seµÃzar sair¡Ãv rop ritsixe medop oitar sihT .ten eht no etalumucca nac egrahc hcum woh stimil suht dna etartsbus eht ot ten eht morf wolf ot snortcele swolla edoid eht ,sneppah siht nehW .)gnihsiloP lacinahceM-lacimehC n.loot gnituor eht yb dellortnoc ylluf si ti taht si noitresni repmuj fo egatnavda ehT .detartnecnoc si egrahc eht hcihw no aera edixo etag decuder a ro egrahc tcelloc ot aera reul ylevitaler a morftem cides on era ereht hcihw rof snoitautis osla era ereht ereht ceremonies A .004 aera etag ylo)5M ot 1M rof(latem hcae fo oitar mumixam eht ,desu ton si edoid noitcetorp eht nehW .dedoc eb nac taht MBI – seigolonhce T tnerruC emoS rof selur ngise D htgnel lennahc rotsisnart detcennoc :l htdiw lennahc rotsisnart detcennoc :2W ssenkciht latem :t etag ot detcennoc htdiw latem gnitaolf :1W etag ot detcennoc htgnel latem gnitaolf taga l*2W/]t*)1W+L(2 = oitaR annetnA .reyal taht woleb melborp annetna yna gnidiova ,reyal tsehgih eht in tpecxe ,aera eriw fo tnuoma llams a ot detcennoc si nip eht hornStates on how much floating load a transistor gate can handle specifying how much wire can be connected to the entrance of the £ £ £ £ £ o before antenna problems occur. We are discussing these two moms here in detail. Mother proposal of field permmetrian field design for the poly -active portion connected directly to it 200. Higher tuning current means higher damage. The insertion of the diode apions the placement and the route connects diodes only to these layers with antenna violations. Plasma charging damage refer to the stress of high field in the intentional port of the door to the mosfet during plasma processing. The insertion of the jumper breaks a long wire so that the connected wire is shorter and less capable of collecting load as shown in the figure. Using diodes to provide a discharge path to the substrate by contact with a diffusion area. In addition, unwanted things happen only because of vain plasma processing steps. There are two points in the design flow, where you can insert diodes to correct antenna violations. As more metal is exposed, the mother load that accumulates in the network that the metal is part also increases. The load-watery is affected by: diffusion path is an np diode for substrate in the drain/source of any hall pin during the plasma-yet that this diode is reversed and, at high temperature gate_area == largest port Lid Size increases the reduction of tension prevents' the diffusion diffusion area from being a great resistance lower than smaller rings the longer wire length acts act as antennas as antennas to "choose" more charge the conditions that lead to antenna formation depend on the technology used to manufacture the chip and must be empirically for each process. It occurs during the manufacturing process and makes it useless. useless. diode insertion is not feasible in regions with very high placement utilization. The other way to repair is to "break up" the antenna by shifting briefly to a different metal. Inserting Diodes Before Detailed Placement Normally, the diode is added only to the pins that need it. In addition, processing steps utilizing plasma can be optimized to reduce the build-up of charges on any antennas that do exist on devices. Antenna repair is accomplished by inserting a reverse-bias diode on the violating net as close to the gates being protected as practical. The wire area as detected by the input pin of the first net is significant, and, therefore, the antenna ratio is exceeded. In these cases, diode insertion is a viable choice. Poly antennae larger than 100 are NOT ALLOWED Floating gate devices with metal antennae larger than 150 are NOT ALLOWED Every N-well is required to be tied down by a N+ diode Antenna Rules: In most cases, antenna rules are in the form of: (antenna-area) / (gate-area) < (max-antenna-ratio) Gate-area Boolean AND of the ¢ÃÂÂpoly¢ÃÂÂ and the ¢ÃÂÂdiffusion¢ÃÂÂ layers Recognized as gate area of the transistors by essentially all foundries Antenna-area Amount of metal area attached to the input pin Calculation method varies for different processes Max-antenna-ratio Represents max allowed ratio of antenna area to gate area Calculation method varies for different processes There are 2 ways to calculate antenna area: Side-Wall Area = (W + L) * 2 * Thickness Polygon Area = W * L Calibre antenna rules M6_DIO = NET AREA SD >= 0.16 A.R.4_A.R.6.M6 { @ (M6 area / gate area + ACCUMULATE) > (600 in OD2, 5500 not in OD2) (without effective diode) @ (M6 area / gate area)+ ACCUMULATE > Ratio (with effective diode) NET AREA RATIO M6 M6_DIO HV_GATE GATE > 0 ACCUMULATE ACC_M5 [!!AREA(M6) * !!AREA(GATE) * (!AREA(M6_DIO)*(!!AREA(HV_GATE)*(AREA(M6)/AREA(GATE)-600) + !AREA(HV_GATE)*(AREA(M6)/AREA(GATE)-5500)) + -(! Ã Rea (m6)+! Ã (gate)) * Largenumber]} ACC_M6 = Razan of the Oge Wool M6 Gate> = 0 Accumula ACC_M5 Magma Antenna Rules: Antenna Rule Metal_rule -Aea_Type ã -Acumulation_Type Path \ -Ratios {{{0 600 0} {0.16E -12 43072.96 456E12}}}} Synopsys Antenna Rules: define_antenna_rule \ -Diode_mode \ Dimode_mode \ -Metal_ratio \ -Cay_Ratia v0 v1 v2 v2 v3 [v4]}> Summary: During the IC manufacturing process, the metal layer is exposed to conditions that lead to an electrosta load. TICA. For this reason, it is important that the saaed pin has some ability to resolve antenna violations. Plasma is an ionized/reactive gene to record. Jumper tons are all more effective to avoid antenna effects problems. Design rules for some current technologies - the metal antenna relationship TSMC 0.18um is not cumulative. cumulative.

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